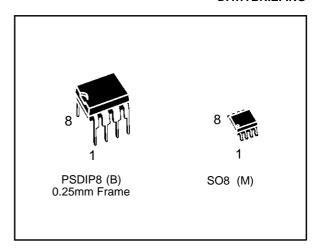


# SERIAL ACCESS SPI BUS 4K (512 x 8) EEPROM

### **DATA BRIEFING**

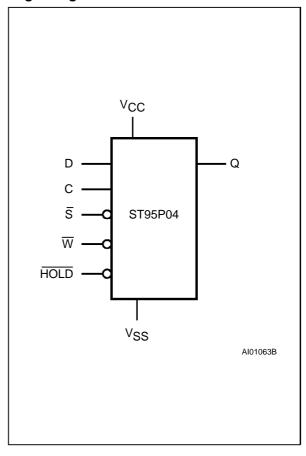
- 1 MILLION ERASE/WRITE CYCLES
- 40 YEARS DATA RETENTION
- SINGLE 3V to 5.5V SUPPLY VOLTAGE
- SPI BUS COMPATIBLE SERIAL INTERFACE
- 1 MHz CLOCK RATE MAX
- BLOCK WRITE PROTECTION
- STATUS REGISTER
- 16 BYTE PAGE MODE
- WRITE PROTECT
- SELF-TIMED PROGRAMMING CYCLE
- E.S.D.PROTECTION GREATER than 4000V
- The ST95P04 will be replaced shortly by the updated version ST95040



### **DESCRIPTION**

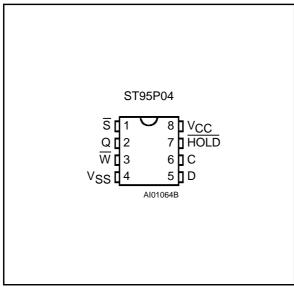
The ST95P04 is a 4K bit Electrically Erasable Programmable Memory (EEPROM) fabricated with SGS-THOMSON's High Endurance Single Polysilicon CMOS technology. The 4K bit memory is organised as 32 pages of 16 bytes. The memory is accessed by a simple SPI bus compatible serial interface. The bus signals are a serial clock input (C), a serial data input (D) and a serial data output (Q). The device connected to the bus is selected when the chip select input  $(\overline{S})$  goes low. Communications with the chip can be interrupted with a hold input  $(\overline{HOLD})$ . The write operation is disabled by a write protect input  $(\overline{W})$ .

## **Logic Diagram**



B95P04/606 1/2

## **DIP Pin Connections**



**Signal Names** 

D

Q

 $\overline{s}$ 

 $\overline{\mathsf{W}}$ 

HOLD

 $V_{CC}$ 

Vss

# **Ordering Information Scheme**For a list of available options refer to the current Memory Shortform catalogue.

For further information on any aspect of this device, please contact the SGS-THOMSON Sales Office nearest to you.

Serial Clock

Chip Select

Write Protect

Supply Voltage

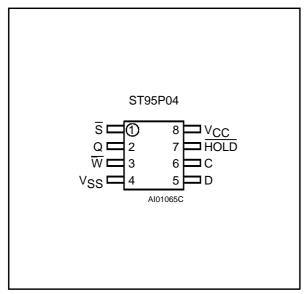
Hold

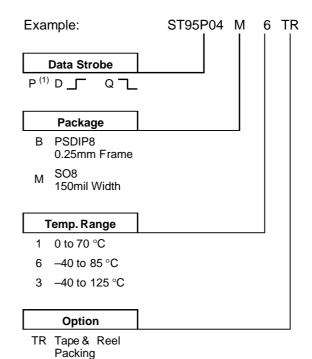
Ground

Serial Data Input

Serial Data Output

## **SO Pin Connections**





Note: 1. Data In strobed on rising edge of the clock (C) and Data Out synchronized from the falling edge of the clock.